REMARKS

Reconsideration of the above-identified patent application is requested in view of the remarks that follow.

This reply is responsive to the July 25, 2002, Final Rejection of this application.

As previously stated by Applicant, a key feature of the semiconductor integrated circuit wafer scale structure claimed as Applicant's invention is the utilization of a unitary, substantially planar, solid glass sheet having substantially the same size as the wafer substrate and having a plurality of prefabricated holes formed therethrough. That is, as recited in Applicant's new claims 68-76, the wafer-sized solid glass sheet is itself prefabricated as a monolithic planar element that has a pattern of prefabricated holes formed, i.e. the holes are formed in the monolithic glass sheet prior to attachment of the solid glass sheet to the semiconductor wafer substrate. Affixation of the solid glass sheet to the wafer substrate aligns the pattern of prefabricated holes in the solid glass sheet with associated die bond pads associated with each of the individual integrated circuit die that are formed on the semiconductor wafer. This facilitates the formation of a solder ball bond pad structure that extends from the upper surface of the solid glass sheet through the solid glass sheet and through adhesive material disposed between the solid glass sheet and the wafer substrate to provide an electrical connection between a conductive solder ball formed on the solder ball bond pad structure and an associated die bond pad formed on the integrated circuit die.

Applicant submits that nothing in the prior art cited by the Examiner to date either teaches or suggests a wafer scale integrated circuit structure that includes a prefabricated unitary, substantially planar solid glass sheet having a plurality of prefabricated holes formed therethrough. To further emphasize this fact, Applicant has recited in new claims 68-76 that the upper and lower surfaces of the glass sheet are coplanar to emphasize its prefabricated nature. All of the references cited by the Examiner either fail completely to disclose glass material "glued" to the "circuit face" of an integrated circuit wafer scale structure, or disclose the application of a glass material to a substrate in manner such that the glass "flows" to conform to

For eaxample, the Examiner refers to the Kata et al. reference as showing a wafer scale device with the wafer connected through film 64 to bumps 70. The film 64 in the Kata et al. structure is recited in the specification of the '304 patent as being a polyimide film applied to have a thickness of 20 micrometers or smaller. The Kata et al. structure also includes a passivating film 12 formed between the covering coating film 64 and the wafer 10. In addition to failing to disclose a monolithic glass sheet having coplanar upper and lower surfaces, which, discussed above, is "glued" to the upper surface of a wafer using adhesive, the Kata et al. reference also fails to disclose an interconnect structure as recited in Applicant's claims.

The Examiner then refers to the Lin reference as showing a flip chip device with a semiconductor chip 12 attached to an interposer board 22. The Examiner states that Lin shows the interposer board attached to a PC board with a layer of adhesive 36, but does not show a similar attachment between semiconductor die 12 and rigid interposer 22. That is, the Examiner is now referring to a reference that is devoid of any discussion of a wafer level semiconductor integrated circuit structure having a momolithic wafer-scale glass sheet affixed to a semiconductor wafer utilizing an adhesive. That is, the Examiner is relying on structure that is not similar to that claimed by Applicant's invention, in that there is no adhesive material between the interposer board 22 and semiconductor chip 12, to obviate claims that are directed to a wafer scale structure.

The Examiner then cites the Tsukamoto et al. reference as teaching an "intermediate substrate" ceramic glass plate 3 in a flip-chip structure. However, the ceramic 3 is not affixed to semiconductor wafer utilizing an adhesive material.

The Igarashi et al. reference is cited as teaching use of polyimide to bond a die to an intermediate sheet. However, the polyimide resin in die-size structure disclosed by Igarashi et al. "encapsulates" the die and is thus not comparable to the wafer-scale layer of adhesive material recited in applicant's claims, since it is not a monolithic structure having coplanar upper and lower surfaces.

The Feldner et al. reference is cited by the Examiner as showing particular features of a chip scale device. However, these feature do not include a prefabricated monolithic glass sheet having a prefabricated pattern of holes formed therein and having coplanar upper and lower

For the record, applicant again submits that the reference combination cited by the Examiner is improper as lacking proper motivation to combine the references in the way suggested by the Examiner, and is a combination arrived only through the use of impermissible hindsight analysis based upon applicant's disclosure.

For the reasons set forth above, Applicant is of the good faith belief that all claims now present in this application are in compliance with all requirements of 35 U.S.C. §112 and patentably distinguish over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

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